WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an insulating layer having a surface in which a plurality of grooves having different widths are formed; and

a conductive layer formed by filling the inside of each of said grooves with at least plating,

wherein unevenness is formed on a bottom portion of each of some grooves among said plurality of grooves.

2. The semiconductor device according to claim 1, wherein said unevenness is formed on a bottom portion of a groove that has a ratio of the depth to the width of not more than 0.7.

3. The semiconductor device according to claim 1, wherein said unevenness is formed on a bottom portion of a groove that has a ratio of the depth to the width of not more than 0.35.

4. The semiconductor device according to claim 1, wherein the concave portion of said unevenness has a groove shape, and said concave portion has a ratio of the depth to the width of greater than 0.35.

5. The semiconductor device according to claim 1, wherein the concave portion of said unevenness has a groove shape, and said concave portion has a ratio of the depth to the width of greater than 0.7.

6. The semiconductor device according to claim 1, wherein the concave portion of said unevenness has a hole shape, and said concave portion has a ratio of the depth to the aperture diameter of greater than 0.35.

7. The semiconductor device according to claim 1, wherein the concave portion of said unevenness has a hole shape, and said concave

8. The semiconductor device according to claim 1, wherein the concave portion of said unevenness has slanting side faces with the two side faces crossing each other in its cross-section.

9. The semiconductor device according to claim 8, wherein the side face of said concave portion is slanted with an angle greater than 20 degrees against an upper surface of said insulating layer.

10. The semiconductor device according to claim 1, wherein the pitch of said concave portions of said unevenness is set to be not more than 4 times the width or the aperture diameter of the concave portion.

11. A manufacturing method of a semiconductor device comprising: the steps of:

forming a plurality of grooves having different widths on a surface of an insulating layer, and forming unevenness on a bottom surface of each of some grooves among said plurality of grooves;

depositing a metal film on said insulating layer by plating so as to be embedded in said plurality of grooves and said unevenness; and

removing said metal film by chemical mechanical polishing until at least the upper surface of said insulating layer is exposed so that said metal film is allowed to remain in said grooves and said unevenness to form a interconnection layer.

12. The manufacturing method of a semiconductor device according to claim 11, further comprising the steps of:

forming a lower interconnection layer as a lower layer beneath said insulating layer; and

forming a connection hole for connecting said lower interconnection layer and said interconnection layer in said insulating layer,

wherein, prior to the formation of said grooves, said connection hole and said unevenness are simultaneously formed.